REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1, 3-13, and 15-16 are pending in the current application. No claims have been canceled, amended, or added.

Claims 1, 3-13 and 15-16 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,875,308 of Egan et al. ("Egan"). Applicant respectfully traverses the rejection.

Claim 1 sets forth a bus bridge device including an internal logic unit, where the bus bridge device is to disconnect the internal logic unit from the bus in response to an assertion of the fault signal. In contrast, Egan fails to disclose such a bus bridge device. The Examiner cited the following passages from Egan to argue that Egan disclosed such a bus bridge device:

> PCI host bus 26 is coupled to a PCI local bus 20 via a PCI local bridge 25. PCI host bridge 11 and PCI local bridge 25 provide a low latency path through which processor 12 may directly access PCI devices mapped anywhere within bus memory and/or I/O address spaces. PCI host bridge 11 and PCI local bridge 25 also provide a high bandwidth path allowing PCI masters direct access to DRAM 15. PCI host bridge 11 and PCI local bridge 25 may include various functions such as data buffering/posting and arbitration. (Egan, col. 3, lines 1-11).
>
> Furthermore, a PCI hot-plug bridge 21 is also coupled to latches 25. As a preferred embodiment of the invention, PCI hot-plug bridge 21 is coupled to latches 25 via five different I/O pins, namely, Power-on Reset 31, Load Clock 32, Shift Clock 33, Data In 34, and Data Out 35. Each of respective pins 31-35 is for latch-up, reading, or driving Service Indicators and Power Control Circuits on a

per-adapter slot basis. On the other hand, the outputs of latches 25 are: 8 outputs for FET control, one per adapter slot; 8 outputs for LEDs, one per adapter slot; 8 inputs for detecting power good, one per adapter slot; 8 inputs for detecting power fault, one per adapter slot; 16 outputs for detecting adapter card present, two per adapter slot. (Egan, col. 3, lines 47-60).

Egan does not disclose that the latches 25 are not an internal logic unit of the PCI hot-plug bridge 21 (see also Figure 2 in Egan) and the latches 25 in Egan are not disconnected from the secondary busses 27a-27h in response to an assertion of a fault signal. Egan merely discloses a FET control 36 to instruct FETs 41 to turn power on or off for adapter slot 29a. The Examiner further argued that it is inherent that once the power failure signal is detected, "the internal logic circuit would be disconnected in protecting any damage to its devices, and other related connected to the device" (Office Action, p. 5, second paragraph). Applicant respectfully disagrees with the Examiner's argument. Claim 1 recites "the bus bridge device to disconnect the internal logic unit **from the bus** in response to an assertion of the fault signal" (emphasis added). It is not inherent to disconnect the internal logic unit from the bus because protecting the internal logic unit from damages caused by power failure is not the reason to disconnect the internal logic unit from the bus in the current application. The internal logic unit is disconnected from the bus in response to a power failure so that the internal logic unit does not become corrupted with invalid data from the bus (see Specification, p. 5, lines 17-20). Since Egan lacks at least the limitations discussed above, Egan fails to anticipate claim 1. Applicant respectfully requests withdrawal of the rejection.

For at least the reason discussed above with respect to claim 1, Egan fails to anticipate claims 10 and 13. Therefore, Applicant respectfully requests withdrawal of the rejection.

Claims 3-9, 11-12, and 15-16 depend, directly or indirectly, from claims 1, 10, and 13, respectively. For at least the reason discussed above with respect to claims 1, 10, and 13, Egan fails to anticipate claims 3-9, 11-12, and 15-16. Applicant respectfully requests withdrawal of the rejection.

Applicant respectfully submits that the rejections have been overcome by the remarks, and that the pending claims 1, 3-13, and 15-16 are in condition for allowance and such action is earnestly solicited.

If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,
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